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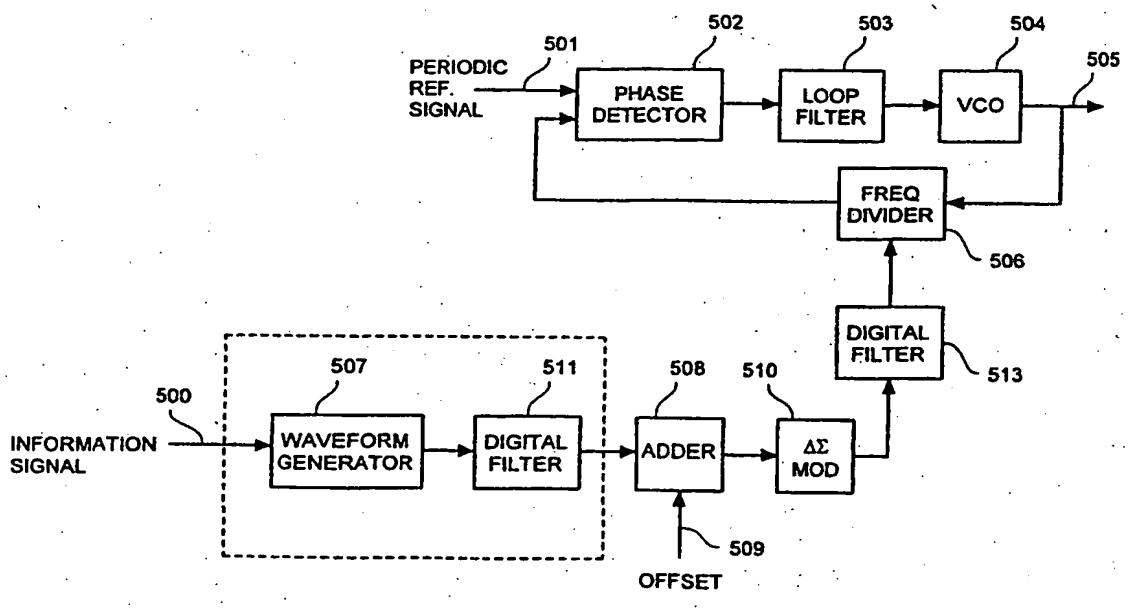

(57) Abstract

A frequency synthesizer has a phase locked loop, a ΔΣ modulator, and a filter. The phase locked loop includes a frequency divider that controls the frequency of the phase locked loop output signal. The output of the ΔΣ modulator is fed through the filter and the output of the filter is used to control a division factor in the frequency divider. Compensation may be performed at the input to the ΔΣ modulator in order to compensate for the filtering performed between the ΔΣ modulator and the frequency divider. The filter may be used to reduce quantization noise in an input to the frequency divider, and thereby reduces phase noise in an output of the phase locked loop.

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A POST-FILTERED ΔΣ FOR CONTROLLING A PHASE LOCKED LOOP MODULATOR

Field of the Invention

The present invention relates to all areas where a ΔΣ controlled phase locked loop (PLL) is used as a frequency synthesizer and/or to generate a phase modulated signal. This applies, for instance, when using a PLL to generate continuous phase modulation (CPM), frequency shift keying (FSK) or quadrature amplitude modulation (QAM) by controlling a division factor in the PLL by means of a ΔΣ modulator. This technique can, for instance, be used in cellular, cordless satellite terminals and base stations.

Background of the Invention

The implementation of continuous phase modulation in a transceiver has traditionally relied on using quadrature modulators. As illustrated in Figure 1, a digital signal processing unit 101 receives the information to be transmitted by a signal 100 and generates the in-phase and quadrature components of the signal. These components are converted to analog signals using digital/analog converters 102a and 102b, and low pass filters 103a and 103b. The output of each filter modulates using multipliers 104a and 104b, one of two carriers 105a or 105b that are separated by 90° in phase. The outputs of the multipliers are then summed in an adder 106 to form the signal 107 which is to be amplified and transmitted.

Recently, continuous phase modulation based on using a ΔΣ modulator to control the division factor of a fractional-N phase locked loop was proposed by Rilev et al. in "A Simplified Continuous Phase Modulation Technique," IEEE Transaction on Circuits and Systems - II: Analog and Digital Signal Processing, Vol. 41, pp. 321-326, May 1994. Phase locked loop frequency synthesis is a well-known technique for generating one of many related signals from a frequency variable voltage controlled oscillator (VCO). In a phase locked loop (PLL), an output signal from the VCO is coupled to a programmable frequency divider which divides the frequency of the PLL output by a selected number (the "division factor") to generate a

frequency divided signal that is supplied to one input of a phase detector. The phase detector compares the frequency divided signal to a reference signal supplied by another fixed frequency oscillator, which, often, is selected for stability of frequency over time and environmental changes. Any difference in phase between the frequency divided signal and the reference signal is output from the phase detector, coupled through a loop filter, and applied to the VCO in a manner which causes the output signal from the VCO to change in frequency such that the phase error between the frequency divided signal and the reference signal is minimized. With a constant division factor, the output frequency step size is constrained to be equal to the reference signal frequency. With the phase locked loop, an engineering compromise must be struck between the competing requirements of loop lock time, output frequency step size, noise performance and spurious signal generation.

In order to overcome the limitations of the PLL, programmable frequency dividers capable of effectively dividing by non-integers have been developed. Output frequency step sizes which are fractions of the reference signal frequency are obtained while maintaining a high reference frequency and wide loop bandwidth. The synthesizers are known as fractional-N frequency synthesizers. Furthermore, a $\Delta\Sigma$ modulator can be used to control the frequency divider of the phase locked loop. Characteristics of a $\Delta\Sigma$ modulator are such that the quantization noise at its output tends to be toward the high end of the spectrum. The $\Delta\Sigma$ modulator is a quantizer that uses feedback to reduce the quantization noise in a limited frequency band. For this application, the $\Delta\Sigma$ modulator should preferably have low quantization noise within the bandwidth of the modulation.

As illustrated in Figure 2, a conventional $\Delta\Sigma$ controlled phase locked loop can be described as consisting of two parts: a $\Delta\Sigma$ modulator 201 and a PLL 202. The output of the $\Delta\Sigma$ modulator 201 is used to control the division factor of a frequency divider in the PLL 202. A more detailed diagram of a conventional $\Delta\Sigma$ controlled phase locked loop modulator is illustrated in Figure 3. A periodic reference signal 301 of frequency f_{ref} is fed to a phase detector 302 together with the phase of the output of the frequency divider 306. The output of the phase detector 302 is a pulse that is related to the phase difference between the reference signal and the output of

the frequency divider 306. The output of the phase detector 302 is filtered through a loop filter 303 and fed to a voltage controlled oscillator 304. Due to the feedback in the phase locked loop, the frequency of the output 305 of the VCO 304 is driven to equal the reference frequency multiplied by the division factor of the frequency divider 306. Hence, the frequency and the phase of the output of the VCO 304 can be controlled by controlling the division factor. In the $\Delta\Sigma$ controlled phase locked loop modulator, the division factors are generated by using a $\Delta\Sigma$ modulator 310. The division factor of the frequency divider can be changed once every period of the reference frequency. The wave generator 307 generates, based on the information signal 300, the input to the $\Delta\Sigma$ modulator 310. Channel selection can be performed by adding in an adder 308, an offset 309 to the input of the $\Delta\Sigma$ modulator 310. The output of the $\Delta\Sigma$ modulator 310 is then used to control the division factor in the frequency divider 306.

The output of the waveform generator is the instantaneous frequency of the desired modulated signal divided by the reference frequency and sampled at the rate of the reference frequency. The oversampling factor, η, of the $\Delta\Sigma$ controlled phase locked loop modulator is

$$\eta = f_{ref}/\text{symbol rate}.$$

The input to the $\Delta\Sigma$ modulator is the instantaneous frequency of the desired modulated signal sampled at a rate equal to f_{ref}. The reference frequency f_{ref} is chosen high enough and the bandwidth of the PLL wide enough for the modulation to fulfill the spectrum and/or the phase noise requirement on the modulation.

Because the phase locked loop is a low pass filter, with respect to the instantaneous frequency, the phase locked loop can be regarded as a means for reconstruction of the desired modulation signal. By choosing the bandwidth of the phase locked loop sufficiently high for the desired modulation to pass, the output of the VCO consists of a signal corresponding to the desired instantaneous frequency and phase noise corresponding to the quantization noise of the $\Delta\Sigma$ modulator. The phase noise can be reduced by either increasing the oversampling factor or by increasing the roll-off of the filtering performed by the phase locked loop. The latter is difficult without jeopardizing the stability margins of the phase locked loop. As a result, prior

systems must rely on the use the high oversampling factors. However, a ΔΣ controlled phase locked loop modulator has many benefits. For example, it enables a cost and space efficient implementation, and guarantees that continuous phase in the modulation as well as channel selection can be controlled in a purely direct and digital manner.

In a mobile station and terminals in cordless cellular and satellite communication systems, or in any other equipment with limited power supply, it is desired to keep the oversampling factor of the PLL as low as possible. With a limited oversampling factor, however, the technique of ΔΣ controlled PLL modulation will fail the spectrum and/or the phase noise requirement on the modulation. This is because the filtering by the PLL will not be able to sufficiently filter the quantization noise without distorting the modulation. Thus, there is a need for a method and apparatus for reducing the amount of quantization noise in the signal applied to the frequency divider from the ΔΣ modulator.

Summary of the Invention

The present invention includes filtering the output of the ΔΣ modulator and using the filtered output to control the division factor of a phase locked loop. Filtering the output of the ΔΣ modulator reduces the quantization noise in the signal used to control the frequency divider. This, in turn, reduces the phase noise in the output of the phase locked loop. According to one embodiment of the present invention, a frequency synthesizer containing a phase locked loop, a ΔΣ modulator and a filter are disclosed. The output of the ΔΣ modulator is fed through the filter and the output of the filter is used to control the division factor in the frequency divider.

In another aspect of the invention, compensation may be performed at the input to the ΔΣ modulator in order to compensate for the filtering performed between the ΔΣ modulator and the frequency divider.

According to another embodiment of the invention, a continuous phase modulator is disclosed. The continuous phase modulator comprises a phase locked loop comprising detector means responsive to a reference signal and a phase control

signal for generating a control signal that varies in dependence upon the phase difference between the reference signal and the phase control signal. Means responsive to the control signal generate an output signal whose frequency varies in dependence upon the control signal. Divider means divides the output signal to provide the phase control signal, the dividing means having a control input and being operable to vary its division ratio in dependence upon a ratio control signal applied to said control input. $\Delta\Sigma$ modulator means responsive to an information signal and an offset signal provides a ratio control signal. Filter means filters the ratio control signal from the $\Delta\Sigma$ modulator means to reduce quantization noise in the ratio control signal, wherein the filtered ratio control signal adjusts the division ratio of the frequency divider. Adjusting means adjust the information signal prior to its being supplied to the $\Delta\Sigma$ modulator means, wherein the adjustment compensates for the action of the filter means.

Brief Description of the Drawings

The invention will now be described in more detail with reference to the accompanying drawings, in which:

Figure 1 illustrates a prior art quadrature modulator;

Figure 2 illustrates a prior art $\Delta\Sigma$ controlled phase locked loop;

Figure 3 illustrates a prior art $\Delta\Sigma$ controlled phase locked loop for generating CPM;

Figure 4 illustrates a post-filtered $\Delta\Sigma$ modulator for controlling a phase locked loop according to one embodiment of the present invention; and

Figure 5, illustrates a post-filtered $\Delta\Sigma$ modulator for controlling a phase locked loop according to one embodiment of the present invention.

Detailed Description

The present invention relates to all areas where a $\Delta\Sigma$ controlled phase locked loop (PLL) is used as a frequency synthesizer and/or to generate a phase modulated signal. This applies, for instance, when using a PLL to generate continuous phase modulation (CPM), frequency shift keying (FSK) or quadrature amplitude modulation

(QAM) by controlling a division factor in the PLL by means of a ΔΣ modulator. This technique can, for instance, be used in cellular, cordless satellite terminals and base stations.

A post-filtered ΔΣ modulator for controlling a phase locked loop is illustrated in Figure 4. A digital filter 402 is introduced between the ΔΣ modulator 401 and the phase locked loop 403. By filtering the output of the ΔΣ modulator 401, the quantization noise in the output signal produced by the ΔΣ modulator 401 can be reduced within certain frequency regions. The reduction in quantization noise can, in turn, be traded for reduced oversampling rate and/or decreased phase noise. This enables the ΔΣ controlled phase locked loop modulation to be used with a limited oversampling factor.

According to the present invention, a transceiver can be enhanced by using the post-filtered ΔΣ controlled phase locked loop modulator depicted in Figure 5. The phase locked loop consists of a phase detector 502, a loop filter 503, a voltage controlled oscillator 504, and a frequency divider 506. The periodic reference signal 501 of frequency f_{ref} is fed to the phase detector 502 together with the phase of the output of the frequency divider 506. The output of the phase detector 502 is a pulse that is related to the phase difference between the reference signal and the output of the frequency divider 506. The output of the phase detector 502 is filtered through a loop filter 503 and fed to a voltage controlled oscillator (VCO) 504. Due to the feedback in the phase locked loop, the frequency of the output of the VCO 504 is driven to equal the reference frequency multiplied by the division factor in the frequency divider 506. Hence, the frequency of the voltage controlled oscillator 504 can be controlled by controlling the division factor.

In the ΔΣ controlled phase locked loop modulator, the division factors are generated by using a ΔΣ modulator 510 whose output is first filtered by a digital filter 513 before being supplied to the frequency divider 506. The purpose of the digital filter 513 is to reduce the quantization noise in the output signal produced by the ΔΣ modulator 510 within certain frequency regions. The ΔΣ modulator 510 may be any type of ΔΣ modulator, such as one of those described in Steven R. Northsworthy, Richard Schrier and Gabor Temes, Delta-Sigma Data Converters, Theory, Design and

Simulation, IEEE Press 1997. According to this exemplary embodiment, the phase locked loop is designed so as to filter the phase noise sufficiently to fulfill the spectrum and/or the phase noise requirements on the modulation. A waveform generator 507 receives an information signal 500 and generates an input for the $\Delta\Sigma$ modulator 510. Prior to being supplied to the $\Delta\Sigma$ modulator 510, however, the generated input signal is first supplied to a prefilter 511, which predistorts the generated input signal so as to compensate for the distortion caused by the digital filter 513. The predistortion can be implemented by distorting the input of the $\Delta\Sigma$ modulator, that is, the desired instantaneous frequency, or by using a waveform generator where the desired predistortion affects the pulse shaping as defined by the modulation scheme.

Several examples will now be presented to illustrate techniques for designing the filter 513. First, consider a situation in which a $\Delta\Sigma$ controlled PLL is to be used to generate modulation for a mobile communications systems in accordance with the European GSM standards. The waveform generator 507 in this case should perform Gaussian filtering. The output of the PLL will then be a Gaussian Minimum Shift Keying (GMSK) modulated signal distorted by the quantization noise generated in the PLL resulting in phase noise. The most critical part to fulfill in the GSM specification is that the phase noise should be less than -60 dBc/Hz at $\pm$400 kHz. Therefore, reducing the quantization noise at 400 kHz is important. The invention offers a simple solution to this problem, as follows.

Consider a reference signal f_{ref} = 13 MHz, as is often used in GSM. The filter 513 can then be chose such that its impulse response is, for example

$$h(k) = \delta(k) + \delta(k-16), \qquad (1)$$

where $\delta(0) = 1$ and $\delta(k) = 0$ for all $k \neq 0$. Then the digital filter 513 would have a notch at 13/30 MHz. This filter has an attenuation of about 12 dB at 400 kHz and a DC gain of 6 dB. The prefilter 511 should then be the inverse filter of $h(k)$ within the bandwidth of the modulation. For the case described above, it is sufficient for the prefilter 511 to compensate for the DC gain with a prefilter containing only one tap

equal to 1/2. The prefilter 511 could, of course, be included in the filtering of the waveform generator 507.

As another example, consider a situation in which it is important to reduce the phase noise of a frequency synthesizer's PLL at neighboring frequency channels. For GSM this would correspond to having a digital filter 513 with notches at, for example, ±200 kHz, ±400 kHz and ±800 kHz. Where the sampling rate of the reference signal 501 is 13 MHz, this can approximately be achieved by a digital filter 513 having an impulse response

$$h(k) = \delta(k) + \delta(k-31).$$

The prefilter 511 could then be a one-tap filter having a gain of one-half.

Note that the coefficients of the digital filter 513 were chosen such that the output of the digital filter 513 is integer valued as long as its input is integer valued. This is an important feature because the frequency divider 506 can only deal with integer valued division factors. The range of the output is twice the range of the input. This has to be taken into consideration when designing the frequency divider.

From the above two examples, one can draw the following conclusions: The invention offers a simple way to reduce phase noise in the PLL within certain frequency regions. A simple digital filter 513 that is easy to implement and will only consume minor power compared to the ΔΣ modulator can reduce the phase noise of the PLL significantly.

As to the digital filtering in prefilter 511, it can typically be described by the relation

$$N(n) = b_1x(k) + b_2x(k-1) + \ldots + b_{k+1}x(k-n)$$
$$-a_2N(k-1) - \ldots - a_{m+1}N(k-m)$$

where N(n) is the output of the filter used to control the frequency divider in the phase locked loop and x(n) is the output of the ΔΣ modulator. The parameters m, n, a_1, $a_2 \ldots a_m$, a_{m+1} and b_1, $b_2 \ldots b_m$, b_{m+1} can be chosen to give the quantization noise certain properties or reduce the quantization noise. Note, however, that the parameters must be chosen such that the output corresponds to a valid division factor in the frequency divider of the phase locked loop.

Channel selection can be performed by using an adder 508 to add an offset 509 to the input of the ΔΣ modulator 510. The reduction in quantization noise can be traded for reduced oversampling rate and/or decreased phase noise, thus enabling the ΔΣ controlled phase locked loop modulation to be used with a limited oversampling factor.

The choice of the ΔΣ modulator is dependent on the desired application. Higher order ΔΣ modulators, possibly implemented using multiple stage (cascade) structures can be used. To enable channel selection over a wide range, the ΔΣ modulator is preferably implemented as a multi-level ΔΣ modulator. The reference signal 501 is preferably a periodic signal. The output of the VCO forms the signal 505 which is to be amplified and transmitted by the transceiver.

A transceiver which can employ the present invention is illustrated in Figure 6. A reference oscillator 601 provides a reference signal, f_{ref}, which remains relatively constant in frequency over time and in extremes of environment and is applied to a ΔΣ-controlled phase locked loop 603 along with the information to be transmitted. The output of the ΔΣ-controlled phase locked loop 603 is used by both the receiver 605 and the transmitter 607 to produce the local oscillator signal and the modulated transmit signal, respectively. In particular, the ΔΣ-controlled phase locked loop 603 supplies a phase-modulated signal to the transmitter 607, and a carrier signal to the receiver 605. In alternative embodiments, amplitude modulation can additionally be introduced in the transmitter 607 when, for example QAM is used. In this case, information to be transmitted should also be supplied to the transmitter 607. In any case, control over functions of the transceiver, such as channel of operation frequency, is provided by the control logic 609.

It will be apparent to those of ordinary skill in the art that the present invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The present disclosed embodiments are, therefore, intended in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.

What is Claimed is:

1. A frequency synthesizer, comprising:

a phase locked loop comprising a frequency divider;

a $\Delta\Sigma$ modulator for modulating an input signal; and

filter means, wherein the output of the $\Delta\Sigma$ modulator is fed through the filter and the output of the filter is used to control a division factor in the frequency divider.

2. The frequency synthesizer according to claim 1, wherein compensation is performed at an input to the $\Delta\Sigma$ modulator in order to compensate for the filtering performed between the $\Delta\Sigma$ modulator and the frequency divider.

3. The frequency synthesizer according to claim 1, wherein said filter means reduces quantization noise in an input to the frequency divider, and thereby reduces phase noise in an output of the phase locked loop.

4. A continuous phase modulator, comprising:

a phase locked loop comprising:

detector means responsive to a reference signal and a phase control signal for generating a control signal that varies in dependence upon the phase difference between the reference signal and the phase control signal;

means responsive to said control signal for generating an output signal whose frequency varies in dependence upon the control signal; and

means for dividing the output signal to provide the phase control signal, said dividing means having a control input and being operable to vary its division ratio in dependence upon a ratio control signal applied to said control input;

$\Delta\Sigma$ modulator means responsive to an information signal to provide a ratio control signal; and

means for filtering said ratio control signal from said $\Delta\Sigma$ modulator means to reduce quantization noise in said ratio control signal, wherein said filtered ratio control signal adjusts the division ratio of the frequency divider.

5. The continuous phase modulator according to claim 4, further comprising:

means for adjusting the information signal prior to its being supplied to the $\Delta\Sigma$ modulator means, wherein the adjustment compensates for the action of the filtering means.

6. The continuous phase modulator according to claim 4, wherein said filter means reduces quantization noise in an input to the dividing means, and thereby reduces phase noise in an output of the phase locked loop.

7. The continuous phase modulator according to claim 4, wherein a channel selection is performed by adding an offset to the input of the $\Delta\Sigma$ modulator.

8. The continuous phase modulator according to claim 4, wherein said $\Delta\Sigma$ modulator means is a multi-level $\Delta\Sigma$ modulator which allows channel selection over a wide frequency range.

9. A method of synthesizing a signal having a frequency, comprising the steps of:

using a phase locked loop to generate the signal, wherein the frequency of the signal is controlled by a frequency divider in the phase locked loop;

using a $\Delta\Sigma$ modulator to generate a modulated signal;

generating a filtered signal by filtering the modulated signal; and

using the filtered signal to control a division factor in the frequency divider.

10. The method of claim 9, further comprising the step of:

supplying a compensated input signal to the $\Delta\Sigma$ modulator, wherein the compensated input signal is made to compensate for the filtering of the modulated signal.

11. The method of claim 9, wherein the step of generating a filtered signal reduces quantization noise in an input to the frequency divider, and thereby reduces phase noise in an output of the phase locked loop.

FIG. 1
(PRIOR ART)

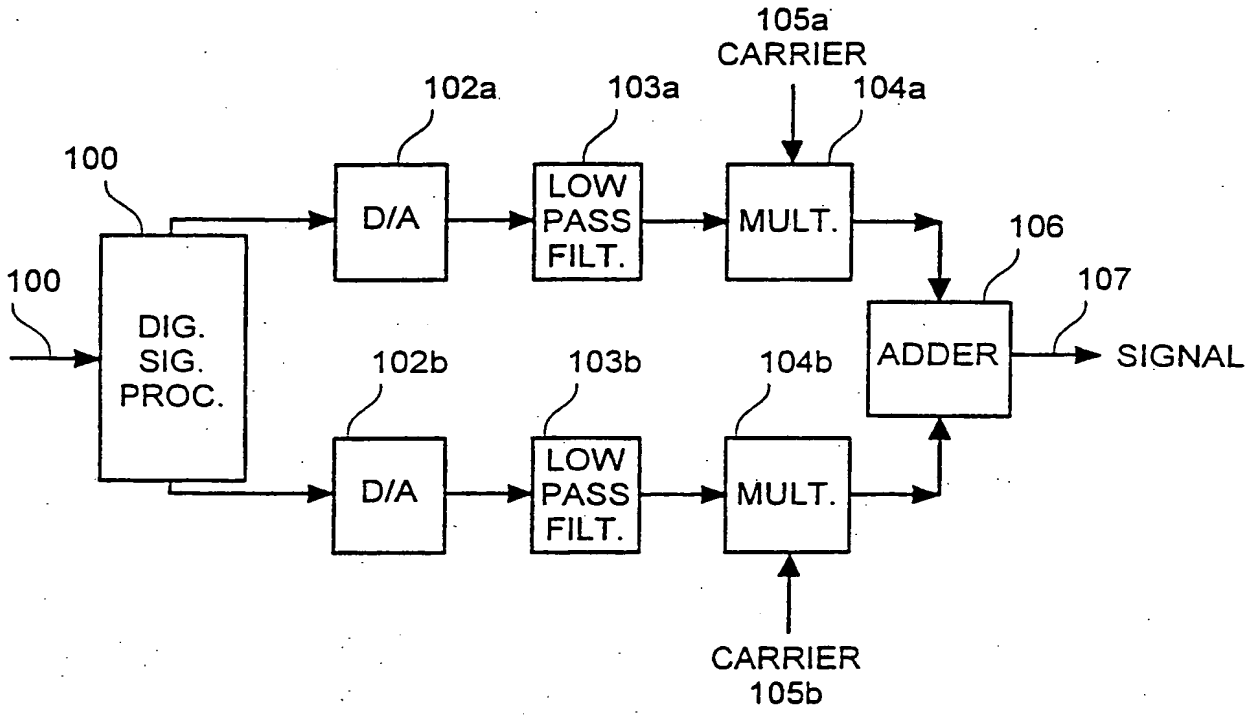
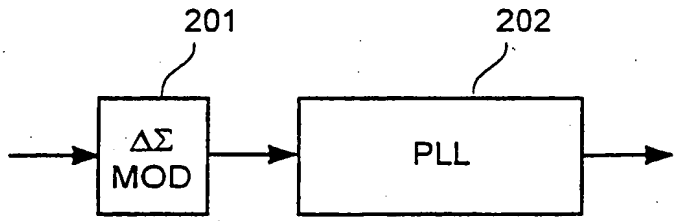


FIG. 2
(PRIOR ART)



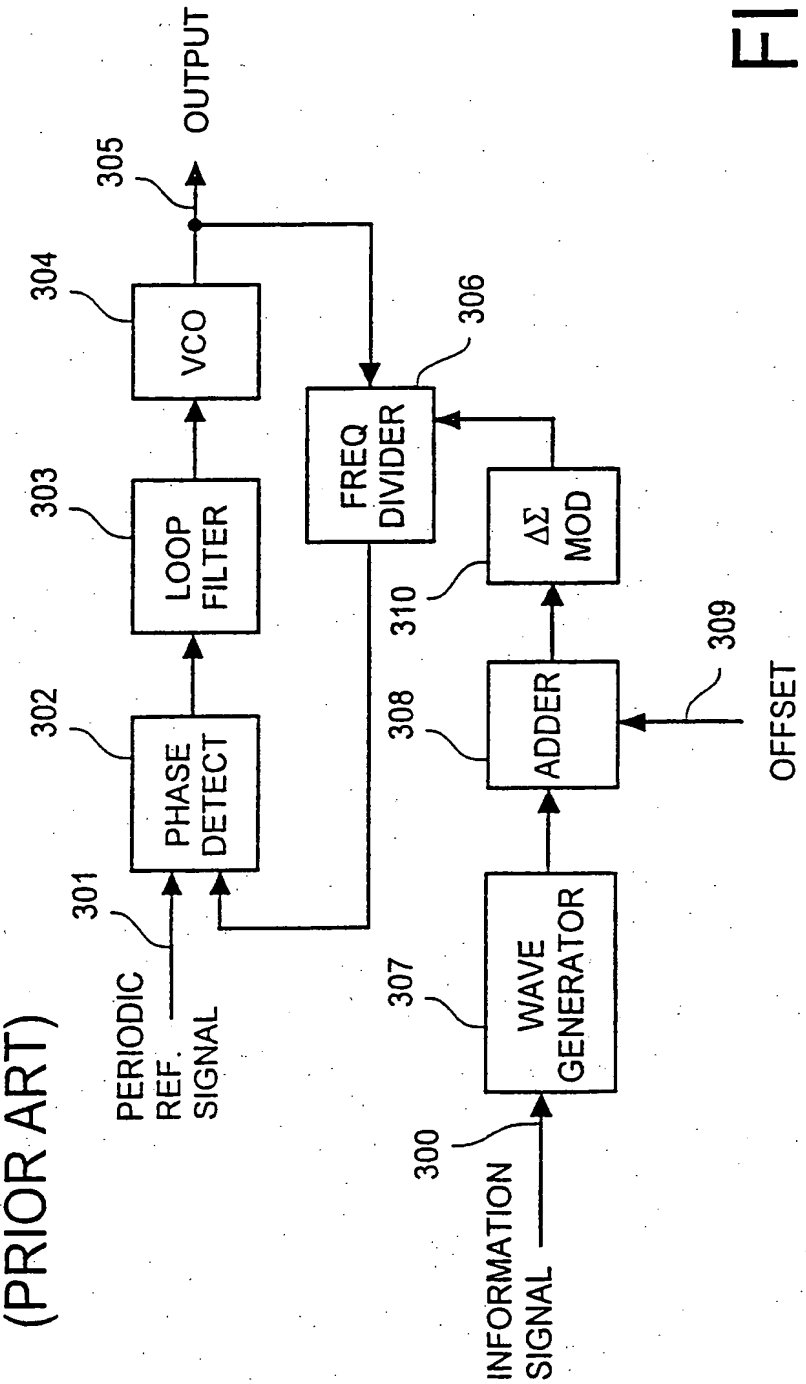


FIG. 3
(PRIOR ART)

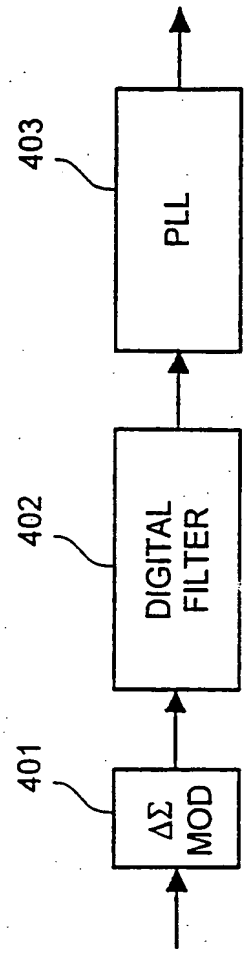


FIG. 4

FIG. 5

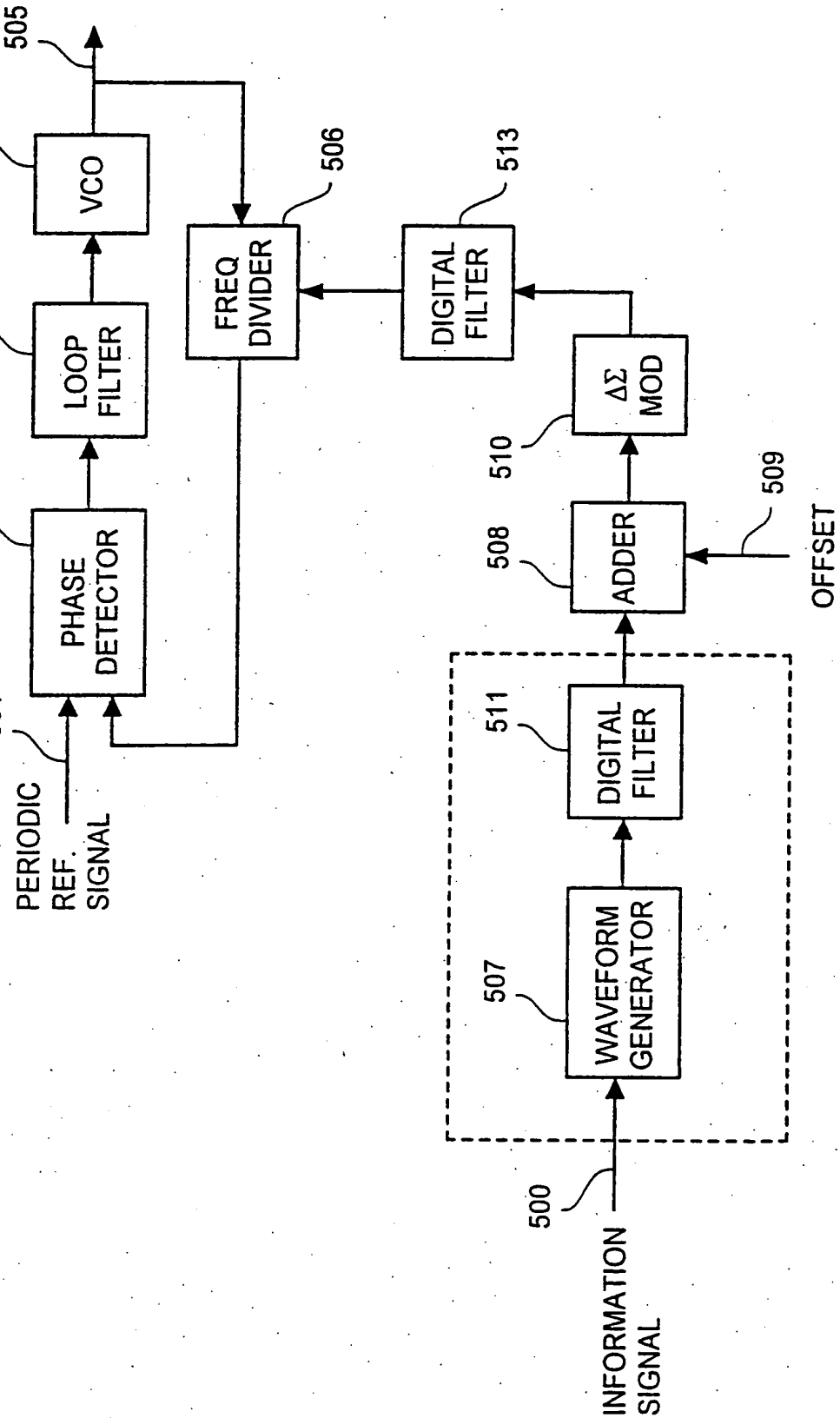
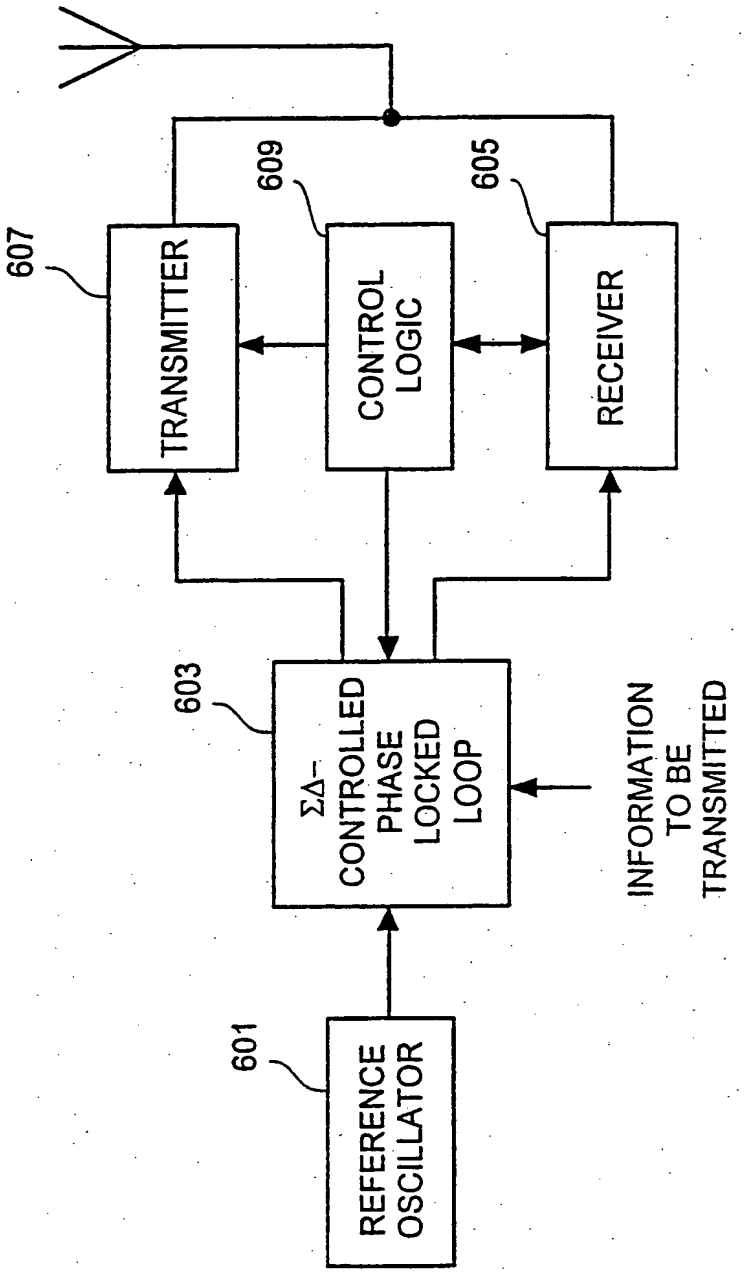

505
504
VCO
506
513
503
LOOP FILTER
FREQ DIVIDER
DIGITAL FILTER
ΔΣ MOD
510
502
PHASE DETECTOR
508
ADDER
509
OFFSET
501
PERIODIC REF. SIGNAL
511
DIGITAL FILTER
507
WAVEFORM GENERATOR
500
INFORMATION SIGNAL

FIG. 6


607
TRANSMITTER
609
CONTROL LOGIC
605
RECEIVER
603
ΣΔ- CONTROLLED PHASE LOCKED LOOP
INFORMATION TO BE TRANSMITTED
601
REFERENCE OSCILLATOR

INTERNATIONAL SEARCH REPORT

Inte .onal Application No
PCT/SE 98/01623

A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03L H03C H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	EP 0 429 217 A (STC PLC) 29 May 1991 see page 3, line 1 - page 4, line 1; figure 6 ---	1,3,6,8, 9,11 2,5,7,10
X	DIAS V D F: "Signal processing in the sigma-delta domain" MICROELECTRONICS JOURNAL, vol. 26, no. 6, September 1995, page 543-562 XP004002165 see page 553, paragraph 4.4 see page 559, paragraph 4.7 see figures 18,22,25 ---	1,3,4,6, 8,9,11
Y	US 5 055 802 A (HIETALA ALEXANDER W ET AL) 8 October 1991 see column 2, line 3 - column 2, line 23 --- -/--	7

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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27 November 1998	07/12/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Kahn, K-D

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International Application No
PCT/SE 98/01623

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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